AMENDMENTS TO THE CLAIMS

Claims 1-3 (canceled)

Claim 4 (presently amended): In a pseudo-random sequence generator having a linear feedback shift register (LFSR) that has a plurality of stages connected so as to generate a first pseudo-random sequence at an output of the last stage of the LFSR and to generate a sequence of vectors each constituting the output of at least some of the stages of the LFSR, a method comprising the steps of:

selectively combining vector values of each vector of the sequence of vectors in a first way to produce a second pseudo-random sequence by exclusive-ORing a first set of vector values of each vector of the sequence of vectors;

~~The method of claim 3, wherein the step of~~ selectively combining vector values of each vector of the sequence of vectors in a second way to produce ~~the~~ a third pseudo-random sequence ~~comprises the step of~~by exclusive-ORing a second set of vector values of each vector of the sequence of vectors, wherein the second set of vector values is different from the first set of vector values; and

selectively outputting bits of the second pseudo-random sequence and at least one bit of the third pseudo-random sequence to form a fourth pseudo-random sequence, wherein the fourth pseudo-random sequence differs from the first pseudo-random sequence.

Claims 5-8 (canceled)

Claim 9 (presently amended): A pseudo-random sequence generator, comprising:

a linear feedback shift register (LFSR) having a plurality of stages, the LFSR generating a first pseudo-random sequence and generating a sequence of vectors each constituting the output of at least some of the stages of the LFSR;

a first mask circuit coupled to receive the sequence of vectors, the first mask circuit generating a second pseudo-random sequence by selectively combining vector values of each vector of the sequence of vectors, wherein the first mask circuit is configured for exclusive-ORing a first set of vector values of each vector of the sequence of vectors to generate the second pseudo-random sequence~~The pseudo-random sequence generator of claim 8~~,

a second mask circuit coupled to receive the sequence of vectors, the second mask circuit generating a third pseudo-random sequence by selectively combining vector values of each vector of the sequence of vectors, wherein the second mask circuit is configured for exclusive-ORing a second set of vector values of each vector of the sequence of vectors to generate the third pseudo-random sequence, where the second set of vector values is different from the first set of vector values; and

logic circuits for generating a fourth pseudo-random sequence from the second pseudo-random sequence and the third pseudo-random sequence, wherein the fourth pseudo-random sequence comprises bits of the second pseudo-random sequence and at least one bit of the third pseudo-random sequence.

Claims 10-22 (canceled)